**PRASEENA N**
prasemanoj@gmail.com
Ph No. 9496401584,04972805918

## SUMMARY

To establish myself in the field of education, to utilize my skills and experience to help students to achieve high improvements in academics. A committed lecturer with over 4.7 years of experience at leading academic institutions, teaching students from various social and cultural backgrounds. Possessing constructive and effective teaching methods along with excellent administrative skills and having the ability to successfully work to tight schedules and deadlines.

## PERSONAL DETAILS

| | |
|---|---|
| Name | : PRASEENA N |
| Date of birth | : 05-08-1979 |
| Present address | : PRASEENA N<br>"SOUPARNIKA"<br>CHERAT, EDAT (P O)<br>KANNUR |
| Gender | : Female |
| BloodGroup | : B+ve |
| Nationality | : INDIAN |
| Contact no | : 9496401584 / 04972805918 |
| Languages known | : English, Hindi & Malayalam |

| ACADEMIC BACKGROUND | | | |
|---|---|---|---|
| **M. Tech (VLSI & Embedded Systems)** | Govt. Model Engineering College, Cochin University of Science and Technology | 85.40% First class with distinction | 2010 |
| **B. Tech (Electronics & Communication Engg)** | LBS College of Engineering, Kannur University | 79.00% First class (Honours) | 2002 |
| **Pre-degree** | Payyanur College, University of Calicut | 82.00% (First class with distinction) | 1997 |
| **Class X** | St. Mary's Girls High school | 92.00% (First class with distinction) | 1995 |

**WORK EXPERIENCE (5 years)**

- **Organization**: Middle East College, Rusayl, Sultanate of Oman
  **Duration**: From October 2013 to June 2014

- **Organization**: Waljat college of Applied Sciences, Rusayl, Oman
  **Duration**: From Feb 2008 to July 2008.

- **Organization:** M.E.S College of Engg. Kuttippuram, Kerala
  **Duration**: From July 2003 to Dec.2005

- **Organization**: Govt. Residential Women's Polytechnic, Payyanur, Kannur, Kerala
  **Duration**: From August 2002 to July 2003

**TECHNICAL SKILLS**

**HDL** : Verilog

**Languages** : C, C++ basic concepts, Assembly language of microprocessors 8085, 8086 and micro controller 8051

**Operating systems**: Windows XP, Linux

**Layout editor** : MAGIC

**Circuit Simulators**: MultiSim,NGSPICE, SPICE, QUCS

## AREAS OF INTEREST

Embedded system design, Digital Electronics

## WORKSHOPS ATTENDED

- Texas Instruments workshop on the Beagle board
- "National Workshop on VLSI Design and Technology" organized by College of Engineering, Cheggannur and Model Engineering College, Thrikkakara in association with IEEE Education Society Chapter

## M. Tech PROJECT

### A STABILITY ENHANCED PRECISION CMOS VOLTAGE REGULATOR FOR BIOIMPLANTABLE APPLICATIONS

- This project is to use CMOS technology to design a voltage regulator circuit for electronic implants.
- Nerve stimulation applications normally need a certain amount of stimulating current. A large voltage supply is required to drive the electrodes. The analog and digital circuitry need to operate from low voltage supplies, in order to minimize their consumed power. In order to maintain long term usability of the implant, efficiency on the power recovery circuitry should be maximized.
- This technique is suitable for providing regulated output voltages to the stimulator output stages and other circuitry.
- No need to carry out surgery for battery replacement or change. This technique is also suitable for bio-telemetry applications which require multilevel output voltages.
- Each of the circuit blocks has been carefully designed under NGSPICE environment. Layout has been drawn using MAGIC layout design tool. From the layout spice netlist has been extracted and that netlist has been simulated in NGSPICE. The extracted simulation results are matching with the original circuit simulation results. The voltage regulator has been verified in a standard 0.35um CMOS process.

## M. Tech SEMINAR

### NULL CONVENTION LOGIC: A COMPLETE AND CONSISTENT LOGIC FOR ASYNCHRONOUS DIGITAL CIRCUIT SYNTHESIS

- Traditional Boolean logic is not symbolically complete because the output of a Boolean gate is

only valid when referenced with time.

- Designers are considering asynchronous circuits as a potential solution to these problems because they are modular and do not require clock synchronization.
- NCL provides an asynchronous design methodology by incorporating data and control information into one mixed path such that there is no need for worst-case delay analysis and control path delay matching.
- NCL eliminates this time-reference problem by employing dual-rail or quad-rail signals. A dual-rail signal 'D' consists of two mutually exclusive wires D0 and D1 which may assume any value from the set {DATA0, DATA1, NULL}

## REFERENCES


- Ms.Pooja Krishnan,Lecturer, Electronics Department, Middle East college, Muscat, Oman, PH: 0096899140851
- Mr. Jagadeesh Kumar P, Senior lecturer, Electronics Department, Model engineering college, Cochin, PH:00919745609827.


## DECLARATION

I hereby declare that the above mentioned particulars are true to the best of my knowledge and belief.

Payyanur

08-03-2022